COMP ENG 2DI4
Logic Design

COURSE OUTLINE
Please refer to course website for updated information.

CALENDAR/COURSE DESCRIPTION

Binary numbers and codes; Boolean algebra; combinational circuit design; electrical properties of logic circuits; sequential circuit design; computer arithmetic; programmable logic; CPU organization and design.

PRE-REQUISITES AND ANTI-REQUISITES

Prereq(s): Registration in a program in Computer Engineering, Electrical Engineering, Engineering Physics (Photonics Engineering Stream) or Physics
Antireq(s): COMPSCI 2MF3, ELECENG 2DI4, SFWRENG 2D03, 2D04, 2DA3, SFWRENG 2DA4

SCHEDULE

Lectures: Every Tuesday, Thursday, Friday 8:30 am – 9:20 am in JHE 376
Tutorials: Every Monday 11:30 am – 12:20 pm in BSB 147 beginning September 9, 2019.
Labs: Every other week 2:30 pm – 5:20 pm beginning September 9, 2019. Note the schedule.

INSTRUCTOR OFFICE HOURS AND CONTACT INFORMATION

Dr. Jennifer Bauman
Email: Jennifer.bauman@mcmaster.ca
Office: ITB-A217
Phone: 905-525-9140 ext. 27784
Office Hours: Every Thursday 1 pm – 2 pm

Ensure your email subject starts with “COE2DI4: “ and include in the body of the message your name, student number, lab section, and lecture section. Please include prior correspondence and endeavour to keep your emails concise. You must send emails from your @mcmaster.ca account.

TEACHING ASSISTANT OFFICE HOURS AND CONTACT INFORMATION

See Avenue to Learn for a drop-in time scheduled in the 2DI4 lab room. This is the time/place to seek help regarding labs and course work. You can also contact a TA for a specific issue. TA names and contact information will be available in the posted lecture notes.

COURSE WEBSITE

The Course Management System (CMS) will be Avenue to Learn. The student is required to **check the system daily** for assignment release/submission, course related material, and posted announcements.

http://avenue.mcmaster.ca/

COURSE OBJECTIVES

By the end of this course, students should be able to:

- Manipulate and simplify Boolean expressions
- Analyze combinational and sequential logic designs
- Synthesize combinational and sequential logic designs
- Design and implement combinational and sequential logic circuits
- Use a hardware description language to implement digital logic design
- Analyze and design digital error detection
- Discuss computer organization in relation to digital systems
- Discuss the impact of digital system design on society

ASSUMED KNOWLEDGE

Successful completion of first year engineering. Students are expected to be proficient in first year engineering mathematics and computation. Students will be required to install course software on their personal computer.

COURSE MATERIALS

All course materials are available through the Titles bookstore or online.

Required items:

1. Textbook: ``*Digital Design: With an Introduction to Verilog HDL, VHDL, and System Verilog*", 6th edition by M. Morris Mano

Optional Items:

1. The following text is recommended as a reference for technical writing – "*Technical Communication: Principles and Practice, Third Edition"* by Raman and Sharma.
2. The following book is suggested to students for supplemental independent reading - ``*Ones and Zeros: Understanding Boolean Algebra, Digital Circuits, and the Logic of Sets*", by John Greg.

Calculator:

No calculator permitted on tests or exams.

COURSE OVERVIEW

Lectures are complemented by the labs and tutorials. To take full advantage of the lecture time, the student must keep up with assigned readings and do the assigned problems. Lectures will be initially focused on theory and then transition into a more balanced theory-application presentation. The lecture time will not be used to teach the software applications (this is done in lab and tutorial). Lectures and labs are mandatory. Tutorials should be considered mandatory. The following is anticipated to be the weekly topic in lecture with associated readings. Based upon the lecture feedback, timing and order may be modified.

Date/Week	Topic
1	Introduction, Number Systems, Boolean Algebra, Logic Gates
2	Gate Level Minimization
3	Combinational Logic: Circuit Analysis and Design, Multiplexers, Adders, Encoders/Decoders
4	Hardware Description Language
5	Synchronous Sequential Logic: Analysis, Latches, Flip-Flops
6	Synchronous Sequential Logic: Analysis, Mealy and Moore Models
	Term Break
7	Synchronous Sequential Logic: Synthesis
8	Synchronous Sequential Logic: Synthesis
9	Digital Systems, Digital Data Error Detection
10	Computer Organization, Memory
11	Register Transfer Level Design
12	Introduction to Assembly
13	Review

Refer to Avenue for assigned reading and questions (2DI4 Schedule). At certain points in the course it may make good sense to modify the schedule. The instructor may modify elements of the course and will notify students accordingly (in class, on the course website).

LABORATORY OVERVIEW

Labs 1-5 have three components: 1) pre-lab assignment/design, 2) in-lab build-test-evaluate, 3) report. Lab session 6 is a practical design and test lab that evaluates a student's ability to

implement combinational and sequential logic circuits. In general, arriving at a lab unprepared will result in an incomplete result. Attendance is mandatory.

When attending labs the student must attend the assigned room and section. Attendance will be taken. **Labs are due at the end of the session.** Penalties for late submission, tardiness, or absence without a valid reason are typically a 0 on the assigned work. A laboratory exercise deemed to be partially or fully copied will be considered an academic offence and be subject to the terms laid out under the McMaster Academic Integrity Policy.

Date/Week	Date/Week	Topic
Sept 9-13	Lab 1 (L02/04/06/08)	Logic Gates
Sept 16-20	Lab 1 (L01/03/05/07)	
Sept 23-27	Lab 2 (L02/04/06/08)	Combinational Logic
Sept 30-Oct 4	Lab 2 (L01/03/05/07)	
Oct 7-11	Lab 3 (L02/04/06/08)	Programmable Logic
Oct 21-25	Lab 3 (L01/03/05/07)	
Oct 28-Nov 1	Lab 4 (L02/04/06/08)	Sequential Logic
Nov 4-8	Lab 4 (L01/03/05/07)	
Nov 11-15	Lab 5 (L02/04/06/08)	Design and Implementation of Synchronous Sequential System
Nov 18-22	Lab 5 (L01/03/05/07)	
Nov 25-29	Lab 6 (L02/04/06/08/07)	Practical Lab
Dec 2-6	Lab 6 (L01/03/05)	

Please be aware of the following penalties for lab and tutorial work:

1. Failure to properly upload and submit your lab evaluation assignment will result in being assigned a 0 for that evaluation. **This means ALL files necessary to evaluate your work**.
2. Failure to submit a lab evaluation assignment by the specified time will result in a 20% penalty up to two minutes late and 100% if more than two minutes.

For example, failure to submit your lab report, code, designs, etc. after completing a lab exercise will result in a grade of 0 for the entire lab (not just a 0 for the marks associated with missing piece(s)).

In terms of submission time, the lab room clock will be the official time. Should the lab room not have a clock or it is unavailable, the TA will specify the reference clock for submission deadlines.

LAB SCHEDULE

Week #	Week Start Date	Lab Exercise	Mon.	Tues.	Wed.	Thurs.	Fri.
1	Sept. 3	No Labs					
2	Sept. 9	1	L02	L04	L06	L08	-
3	Sept. 16	1	L01	L03	L05	L07	-
4	Sept. 23	2	L02	L04	L06	L08	-
5	Sept. 30	2	L01	L03	L05	L07	-
6	Oct. 7	3	L02	L04	L06	L08	-
	Oct. 14	Midterm Recess					
7	Oct. 21	3	L01	L03	L05	L07	-
8	Oct. 28	4	L02	L04	L06	L08	-
9	Nov. 4	4	L01	L03	L05	L07	-
10	Nov. 11	5	L02	L04	L06	L08	-
11	Nov. 18	5	L01	L03	L05	L07	-
12	Nov. 25	Practical Lab	L02	L04	L06	L08	L07
13	Dec. 2	Practical Lab	L01	L03	L05	MSAF	

Note: The Practical Lab for L07 will be held on Nov. 29, 2019 from 2:30-5:30.

ASSESSMENT

Component	Weight
Lab Evaluation	25%
Midterm Exam	25%
Practical Lab	10%
Final Exam	40%
Total	100%

The final exam must be written else a final grade of F will be awarded with the notation DNW (Did Not Write). To pass the course you must obtain at least 50% on the final examination. Statistical adjustments (such as bell curving) will not normally be used. If the midterm is not written, or a student achieves a higher grade on the final exam, the midterm mark will be replaced by the final exam mark.

In a case where the component weight cannot be fulfilled as a result of unforeseen and/or uncontrollable circumstance(s) in the course operation or execution, the grades assigned to that component may be pro-rated.

See Avenue for dates, times, and locations of Midterm Exam and Final Exam.

The instructor reserves the right to choose the format (i.e. written or oral) of any deferred midterm or final exam in this course.

Unless otherwise stated, tests, practical labs, and examinations are closed-book.

Please note that announcements concerning any type of graded material may be in any format (e.g., announcements may be made only in class). Students are responsible for completing the graded material regardless of whether they received the announcement or not. This means that if you skip a class and an announcement for a quiz, lab, test, project, etc. is made in that class, then you are still responsible for that material.

ACCREDITATION LEARNING OUTCOMES

Note: The *Learning Outcomes* defined in this section are measured throughout the course and form part of the Department's continuous improvement process. They are a key component of the accreditation process for the program and will not be taken into consideration in determining a student's actual grade in the course. For more information on accreditation, please ask your instructor or visit: http://www.engineerscanada.ca .

Outcomes	Indicators	Measurement Methods(s)
Demonstrates an ability to identify a range of suitable engineering fundamentals (such as Boolean Algebra, Karnaugh maps, etc.) to analyze and solve for the minimized form of a digital combinational circuit.	2.2	Assess implementation of practical lab circuit
Demonstrates an ability to identify a range of suitable engineering fundamentals (such as State Assignment, State Reduction, etc.) to analyze and solve for the minimized form of a digital sequential circuit.	2.2	Assess implementation of practical lab circuit
Using specialized software and hardware to demonstrate designing, building and troubleshooting digital combinational and sequential circuits.	5.2	Assess HDL implementation of lab 3 circuits
Understand the differences between Mealy and Moore sequential design and be able to correctly choose based upon application.	3.1	Assess design and rationale for implementation of lab 4 circuit
Discuss the local and global implications of sustainability in a digital system design.	9.1	Written response

ACADEMIC INTEGRITY

You are expected to exhibit honesty and use ethical behaviour in all aspects of the learning process. Academic credentials you earn are rooted in principles of honesty and academic integrity. Academic dishonesty is to knowingly act or fail to act in a way that results or could result in unearned academic credit or advantage. This behaviour can result in serious consequences, e.g. the grade of zero on an assignment, loss of credit with a notation on the transcript (notation reads: “Grade of F assigned for academic dishonesty”), and/or suspension or expulsion from the university.

It is your responsibility to understand what constitutes academic dishonesty. For information on the various types of academic dishonesty please refer to the Academic Integrity Policy, located at www.mcmaster.ca/academicintegrity.

The following illustrates only three forms of academic dishonesty:
• Plagiarism, e.g. the submission of work that is not one’s own or for which other credit has been obtained.
• Improper collaboration in group work.
• Copying or using unauthorized aids in tests and examinations.

ACADEMIC ACCOMMODATIONS

Students with disabilities who require academic accommodation must contact Student Accessibility Services (SAS) to make arrangements with a Program Coordinator. Student Accessibility Services can be contacted by phone 905-525-9140 ext. 28652 or e-mail sas@mcmaster.ca . For further information, consult McMaster University’s Academic Accommodation of Students with Disabilities policy.

Students requiring academic accommodation based on religious, indigenous or spiritual observances should follow the procedures set out in the RISO policy. Students requiring a RISO accommodation should submit their request to the Engineering Student Services office normally within 10 working days of the beginning of term in which they anticipate a need for accommodation or to the Registrar's Office prior to their examinations. Students should also contact their instructors as soon as possible to make alternative arrangements for classes, assignments, and tests.

STUDENT ABSENCE AND SUBMISSION OF REQUEST FOR RELIEF FOR MISSED ACADEMIC WORK

In the event of an absence for medical or other reasons, students should review and follow the Academic Regulation in the Undergraduate Calendar “Requests for Relief for Missed Academic Term Work”.

EXTREME CIRCUMSTANCES

The University reserves the right to change the dates and deadlines for any or all courses in extreme circumstances (e.g., severe weather, labour disruptions, etc.). Changes will be

communicated through regular McMaster communication channels, such as McMaster Daily News, A2L and/or McMaster email.

ONLINE ACCESS OR WORK

In this course we will be using Avenue To Learn. Students should be aware that, when they access the electronic components of this course, private information such as first and last names, user names for the McMaster e-mail accounts, and program affiliation may become apparent to all other students in the same course. The available information is dependent on the technology used. Continuation in this course will be deemed consent to this disclosure.
If you have any questions or concerns about such disclosure please discuss this with the course instructor.

RESEARCH ETHICS

The two principles underlying integrity in research in a university setting are these: a researcher must be honest in proposing, seeking support for, conducting, and reporting research; a researcher must respect the rights of others in these activities. Any departure from these principles will diminish the integrity of the research enterprise. This policy applies to all those conducting research at or under the aegis of McMaster University. It is incumbent upon all members of the university community to practice and to promote ethical behaviour. To see the Policy on Research Ethics at McMaster University, please go to http://www.mcmaster.ca/policy/faculty/Conduct/ResearchEthicsPolicy.pdf.

The Department of Electrical & Computer Engineering website:
www.eng.mcmaster.ca/ece

Electrical and Computer Engineering Lab Safety

Information for Laboratory Safety and Important Contacts

This document is for users of ECE instructional laboratories in the Information Technology Building.

This document provides important information for the healthy and safe operation of ECE instructional laboratories. This document is required reading for all laboratory supervisors, instructors, researchers, staff, and students working in or managing instructional laboratories in ECE. It is expected that revisions and updates to this document will be done continually. A McMaster University lab manual is also available to read in every laboratory.

General Health and Safety Principles

Good laboratory practice requires that every laboratory worker and supervisor observe the following:

1. Food and beverages are not permitted in the instructional laboratories.
2. A Laboratory Information Sheet on each lab door identifying potential hazards and emergency contact names should be known.
3. Laboratory equipment should only be used for its designed purpose.
4. Proper and safe use of lab equipment should be known before using it.
5. The course TA leading the lab should be informed of any unsafe condition.
6. The location and correct use of all available safety equipment should be known.
7. Potential hazards and appropriate safety precautions should be determined, and sufficiency of existing safety equipment should be confirmed before beginning new operations.
8. Proper waste disposal procedures should be followed.

Location of Safety Equipment

Fire Extinguisher
On walls in halls outside of labs

First Aid Kit
ITB A111, or dial “88” after 4:30 p.m.

Telephone
On the wall of every lab near the door

Fire Alarm Pulls
Near all building exit doors on all floors

Who to Contact

Emergency Medical / Security: On McMaster University campus, call Security at extension **88** or **905-522-4135** from a cell phone.
Non-Emergency Accident or Incident: Immediately inform the TA on duty or Course Instructor.
University Security (Enquiries / Non-Emergency): Dial 24281 on a McMaster phone or dial 905-525-9140 ext. 24281 from a cell phone.
See TA or Instructor: For problems with heat, ventilation, fire extinguishers, or immediate repairs
Environmental & Occupational Health Support Services (EOHSS): For health and safety questions dial 24352 on a McMaster phone or dial 905-525-9140 ext. 24352 from a cell phone.
ECE Specific Instructional Laboratory Concerns: For non-emergency questions specific to the ECE laboratories, please contact 24103.

In Case of a Fire (Dial 88)

When calling to report a fire, give name, exact location, and building.

1. Immediately vacate the building via the nearest Exit Route. Do not use elevators!
2. Everyone is responsible for knowing the location of the nearest fire extinguisher, the fire alarm, and the nearest fire escape.
3. The safety of all people in the vicinity of a fire is of foremost importance. But do not endanger yourself!
4. In the event of a fire in your work area shout "*Fire!*" and pull the nearest fire alarm.
5. Do not attempt to extinguish a fire unless you are confident it can be done in a prompt and safe manner utilizing a hand-held fire extinguisher. Use the appropriate fire extinguisher for the specific type of fire. Most labs are equipped with Class A, B, and C extinguishers. Do not attempt to extinguish Class D fires which involve combustible metals such as magnesium, titanium, sodium, potassium, zirconium, lithium, and any other finely divided metals which are oxidizable. Use a fire sand bucket for Class D fires.
6. Do not attempt to fight a major fire on your own.
7. If possible, make sure the room is evacuated; close but do not lock the door and safely exit the building.

Clothing on Fire

Do not use a fire extinguisher on people

1. Douse with water from safety shower immediately or
2. Roll on floor and scream for help or
3. Wrap with fire blanket to smother flame (a coat or other nonflammable fiber may be used if blanket is unavailable). Do not wrap a standing person; rather, lay the victim down to extinguish the fire. The blanket should be removed once the fire is out to disperse the heat.

Equipment Failure or Hazard

Failure of equipment may be indicative of a safety hazard - You must report all incidents.

Should you observe excessive heat, excessive noise, damage, and/or abnormal behaviour of the lab equipment:

1. Immediately discontinue use of the equipment.
2. In Power Lab, press wall-mounted emergency shut-off button.
3. Inform your TA of the problem.
4. Wait for further instructions from your TA.
5. TA must file an incident report.

Protocol for Safe Laboratory Practice

Leave equipment in a safe state for the next person - if you're not sure, ask!

In general, leave equipment in a safe state when you finish with it. When in doubt, consult the course TA.

Defined Roles

TA	The first point of contact for lab supervision	
ECE Lab Supervisor	Steve Spencer- ITB 147	steve@mail.ece.mcmaster.ca
ECE Chair	Tim Davidson- ITB A111	davidson@mcmaster.ca
ECE Administrator	Kerri Hastings- ITB A111	hastings@mcmaster.ca
ECE Course Instructor	Please contact your specific course instructor directly	