Cadence Program

Department of Electrical and Computer Engineering, McMaster University
Hamilton, Ontario, Canada

Cadence University Program Member

This page provides information only about the Cadence software used at our university

Cadence Tools in Our Curriculum

Cadence software is being used in the following courses (click each course title below to expand for more details):

Graduate Course - EE740 Semiconductor Device Theory and Modeling

- This course provides a fundamental in-depth knowledge of the theory of operation, modeling, parameter extraction, scaling issues, and higher order effects of active and passive semiconductor devices that are used in mainstream semiconductor technology. There will be a comprehensive review of the latest models for the devices that are. valid out to very high frequencies and the use of physical device modeling/CAD tools. A review of the latest device technologies will be presented.

Graduate Course - EE741, Analog Integrated Circuits

- This course provides a fundamental and in-depth knowledge of the analysis, modeling, and design of analog integrated circuits (ICs), mostly at radio frequencies (RF). It covers many aspects of the analysis and design of analog integrated circuits, mostly in CMOS technology. The topics include transistor models, reliability, smallsignal analysis, amplifier design, biasing, noise analysis, low power design and examples of analog and RF ICs. It includes a review of the important circuit design techniques and device technologies.

Graduate Course - EE746, Analysis and Design of RF ICs for Communications

- This course provides a fundamental and in-depth knowledge of the analysis and design of radio-frequency (RF) integrated circuits (IC) in CMOS technology for wireless communications. The topics include the modeling of active and passive components for AC and noise analysis, design examples of amplifiers, oscillators, PLL and frequency synthesizers. Circuit performance will be evaluated by both hand calculations and computer simulations using Cadence products (e.g., SpectreRF) for custom IC design and verification. A good understanding of circuit analysis and CAD tools is required.

Undergraduate Course - EE/COE 4OJ4 Research Project

- EE/COE 4OJ4 provides a fundamental and in-depth knowledge of the analysis, modeling and design of operational amplifiers in CMOS technology. Cadence design environment is used to design and simulate (using Spectre) the circuits in assignments and a term project.

Undergraduate Course - COE 4EK4 - Microelectronics

- This course is concerned with integrated circuit or chip design, simulation and layout. Specific topics addressed are: CMOS and MOSFET integrated circuit design; fabrication and layout; simulation; digital and analog circuit blocks; computer aided design and analysis; testing and verification. Cadence design environment is used to design and simulate the circuit and generate the layout in assignments and a term project.

Cadence Tools in Our Research

Cadence software was used in the design, layout and/or simulation of the circuits and devices featured in the following publications (click each publication title below to expand for more details):

2015 Publications:

Microwave holography using measured point-spread functions
R.K. Amineh, J. McCombe, A. Khalatpour, and N.K. Nikolova, “Microwave holography using measured point-spread functions,” IEEE Trans. Instrum.&Meas., vol. 64, no. 2, Feb. 2015, pp. 403–417.

Toward Realization of 2.4 GHz Balunless Narrowband Receiver Front-End for Short Range Wireless Applications
El-Desouki, Munir M.; Qasim, Syed M.; BenSaleh, Mohammed S.; Deen, M. J. 2015. "Toward Realization of 2.4 GHz Balunless Narrowband Receiver Front-End for Short Range Wireless Applications." Sensors 15, no. 5: 10791-10805.

2014 Publications:

Sensitivity of microwave imaging systems employing scattering-parameter measurements
K. Moussakhani, J.J. McCombe, and N.K. Nikolova, “Sensitivity of microwave imaging systems employing scattering-parameter measurements,” IEEE Trans. Microwave Theory Tech., vol. 62, no. 10, Oct. 2014, pp. 2447–2455.

Analytical S-parameter sensitivity formula for the shape parameters of dielectric objects

M.S. Dadash and N.K. Nikolova, “Analytical S-parameter sensitivity formula for the shape parameters of dielectric objects,” IEEE Microw. Wireless Comp. Lett., vol. 24, no. 5, May 2014, pp. 291–293.

Wideband second-order adjoint sensitivity analysis exploiting TLM
M.H. Negm, M.H. Bakr, N.K. Nikolova, and J.W. Bandler, “Wideband second-order adjoint sensitivity analysis exploiting TLM,” IEEE Trans. Microwave Theory Tech., vol. 62, no. 3, March 2014, pp. 389–398.

2012 Publications:

Silicon Photonics - Fundamentals and Devices

- M.J. Deen and P.K. Basu, Silicon Phtonics - Fundamentals and Devices, John Wiley and Sons Ltd., ISBN-13: 978-0-470-51750-5, 456 pages (2012). Part of Wiley series in Materials for Electronic and Optoelectronic Applications. The creation of affordable high speed optical communications using standard semiconductor manufacturing technology is a principal aim of silicon photonics research. This would involve replacing copper connections with optical fibres or waveguides, and electrons with photons. With applications such as telecommunications and information processing, light detection, spectroscopy, holography and robotics, silicon photonics has the potential to revolutionise electronic-only systems. Providing an overview of the physics, technology and device operation of photonic devices using exclusively silicon and related alloys, the book includes: Basic Properties of Silicon; Quantum Wells, Wires, Dots and Superlattices; Absorption Processes in Semiconductors; Light Emitters in Silicon; Photodetectors, Photodiodes and Phototransistors; Raman Lasers including Raman Scattering; Guided Lightwaves; Planar Waveguide Devices; Fabrication Techniques and Material Systems. This publication outlines the basic principles of operation of devices, the structures of the devices, and offers an insight into state-of-the art and future developments.

Effects of Gate Oxide and Junction Non-Uniformity on the DC and Low-Frequency Noise Performance of Four-Gate Transistors

- Juan A. Jimenez Tejada, Abraham Luque Rodriguez, Andres Godoy, Salvador Rodriguez-Bolivar, Juan A. Lopez Villanueva, Ognizn marinov, and M. Jamal Deen, "Effects of Gate Oxide and Junction Non-Uniformity on the DC and Low-Frequency Noise Performance of Four-Gate Transistors," IEEE Transactions on Electron Devices, Vol. 59(2), pp. 459-467 (February 2012).

Fabrication of Vertically-Stacked Single-Crystalline Si Nanowires Using Self-Limiting Oxidation

- Tao Wang, Bin Yu, Yan Liu, Qing Guo, Kuang Sheng, and M. Jamal Deen, "Fabrication of Vertically-Stacked Single-Crystalline Si Nanowires Using Self-Limiting Oxidation," Nanotechnology, Vol. 23(1), # 015307, 5 journal pages (13 January 2012).

A Wireless Wearable ECG Sensor for Long-Term Applications

- Ebrahim Nemati, M.Jamal Deen and Tapas Mondal, "A Wireless Wearable ECG Sensor for Long-Term Applications," IEEE Communications Magazine (Special Issue on Communications in Unbiquitous Healthcare), Vol. 50(1), pp. 36-43 (January 2012).

Equivalent Sheet Resistance of Intrinsic Noise in Sub-100nm MOSFETs

- C.H. Chen, R. Lee, G. Tan, D.C. Chen, P. Lei, and C.S. Yeh, "Equivalent Sheet Resistance of Intrinsic Noise in Sub-100nm MOSFETs," accepted by IEEE Trans. ElectronDevices, May 1, 2012.

- This paper presents the equivalent sheet resistance for the intrinsic channel thermal noise of sub-100nm MOSFETs for the first time. This newly defined noise sheet resistance is particularly helpful when comparing the noise performance of devices in different technology nodes for low-noise applications. Experimental results for devices in 130nm, 90nm, and 65nm CMOS technology nodes are demonstrated. Strategies for the development of future low-noise technologies are suggested. Cadence circuit simulator (Spectre) was used to extract the power spectral density of the thermal noise in these three technologies.

2011 Publications:

A Fully Integrated CMOS Power Amplifier Using Superharmonic Injection-Locking for Short-Range Applications

- This work demonstrates the feasibility of using a superharmonic injection-locked oscillator as a power amplifier for short-range, low-power applications. This paper presents two fully integrated, differential superharmonic injection-locked power amplifiers (ILPA) operating at 433 MHz and 2.4 GHz. The two circuits were fabricated in a standard 0.18 ?m CMOS technology. Measurement results of the 2.4 GHz ILPA show a maximum gain of 31 dB from only one stage that occupies a chip area of only 0.6 mm2 with all components fully integrated. The ILPA delivers an output power of 7.6 dBm from a 1.5 V supply voltage with a power added efficiency of 36%.
- Munir M. El-Desouki, M. Jamal Deen, Yaser M. Haddara, and Ognian Marinov IEEE SENSORS JOURNAL, In Press, 2011.

High-Speed, Single-Photon Avalanche-Photodiode Imager for Biomedical Applications

- The design of a low-light level pixel in CMOS technology for biomedical applications is described. This pixel is also suitable for extremely high-speed applications, such as fluorescence lifetime imaging (FLIM) used for drug discovery and/or minimally-invasive optical biopsy. In order to achieve high-speed imaging using single-photon detection, a

detector with a very low dead-time is needed. The single-photon avalanchephotodiode (SPAD) discussed in this work uses a mainstream deep-submicron CMOS technology in order to achieve ultrahighspeed operation and high pixel fill-factor, with in-pixel active quench and reset circuits. The paper also presents an innovative approach for reducing the deadtime of the detector and an attractive technique for simultaneous high-speed image acquisition by all the pixels of an array in parallel.

- Darek Palubiak, Munir M. El-Desouki, Ognian Marinov, M. Jamal Deen, and Qiyin Fang IEEE SENSORS JOURNAL, In Press, 2011.

A Novel, High-Dynamic-Range, High-Speed, and High-Sensitivity CMOS Imager Using Time-Domain Single-Photon Counting and Avalanche Photodiodes

- Avalanche photodiodes used in Geiger mode as single-photon counters have become very attractive imaging tools. High-speed single-photon imaging can be used in very low-light-level applications such as surveillance and security imaging, quantum computing, and biomedical imaging including bioluminescence and fluorescence lifetime imaging. However, a typical avalanche-based single-photon detector cannot offer the high dynamic range that is needed for many biomedical and surveillance applications. In this paper, we show how a single-photon detector can be used in time domain for high-dynamic-range applications. We also discuss novel techniques to implement the time-domain single-photon imager in mainstream deep-submicrometer CMOS technology. The designed imager
  offers high dynamic range and high sensitivity, while maintaining high-speed operation and low cost.
- Munir M. El-Desouki, Darek Palubiak, M. Jamal Deen, Qiyin Fang, and Ognian Marinov IEEE SENSORS JOURNAL, VOL. 11, NO. 4, pp. 1078-1083, APRIL 2011

2010 Publications:

A Dual Continuous and Bust-Mode Clock Recovery Module Utilizing Fiber Dispersion

- A clock recovery module suitable for both burst- and continuous-mode optical receiver utilizing fiber dispersion is experimentally demonstrated for the first time. The module utilizes the nonlinear characteristics of the received nonreturn-to-zero (NRZ) optical signals experiencing the fiber dispersion and the photo-detection to extract the clock information. Experiments demonstrated its functionality in both operation modes up to 9 Gbps.
- M. Yan, C. H. Chen, Q. Y. Xu, and W. P. Huang,"A Dual Continuous and Bust-Mode Clock Recovery Module Utilizing Fiber Dispersion," Microwave and Optical Technology Letters, vol. 52, issue 8, pp. 1747-1750, August 2010.

2009 Publications:

CMOS photodetector systems for low-level light applications

- In this work, we have designed, fabricated and measured the performance of three different active pixel sensor (APS) structures. These APS structures are studied in the context of applications that requirelow-level light detection systems. The three APS structures studied were - a conventional APS, an APS with a comparator, and an APS with an integrator. A special focus of our study was on both the signal andnoise characteristics of each APS structure so the key performance metric of signal-to-noise ratio can be computed and compared. The pixelstructures that are introduced in this work can cover a wide range of applications, such as high resolution digital photography using the APSwith a comparator, to ultra-sensitive biomedical measurements using theAPS with an integrator.
- Invited paper - Naser Faramarzpour, Munir M. El-Desouki, M. Jamal Deen, Shahram Shirani and Qiyin Fang, CMOS photodetector systems for low-level light applications, J Mater Sci: Mater Electron - Special Issue, Vol.20, pp. S87¡VS93 (2009)

CMOS Image Sensors for High Speed Applications

- Recent advances in deep submicron CMOS technologies and improved pixel designs have enabled CMOS-based imagers to surpass charge-coupled devices (CCD) imaging technology for mainstream applications. Theparallel outputs that CMOS imagers can offer, in addition to completecamera-on-a-chip solutions due to being fabricated in standard CMOS technologies, result in compelling advantages in speed and system throughput. Since there is a practical limit on the minimum pixel size(4~5 £gm) due to limitations in the optics, CMOS technology scaling can allow for an increased number of transistors to be integrated into the pixel to improve both detection and signal processing. Such smart pixelstruly show the potential of CMOS technology for imaging applications allowing CMOS imagers to achieve the image quality and global shuttering performance necessary to meet the demands of ultrahigh-speedapplications. In this paper, a review of CMOS-based high-speed imager design is presented and the various implementations that targetultrahigh-speed imaging are described. This work also discusses the design, layout and simulation results of an ultrahigh acquisition rate CMOS active-pixel sensor imager that can take 8 frames at a rate of more than a billion frames per second (fps).
- Review Article, Munir El-Desouki, M. Jamal Deen, Qiyin Fang, Louis Liu, Frances Tse and David Armstrong, CMOS Image Sensors for High Speed Applications, Sensors, Vol 9, pp. 430-444 (2009).

The Impact of On-Chip Interconnections on CMOS RF Integrated Circuits

- Achieving power- and area-efficient fully integrated transceivers is one of the major challenges faced when designing high-frequency electronic circuits suitable for biomedical applications or wireless sensornetworks. The power losses associated with the parasitics of on-chip inductors, transistors, and interconnections have posed designchallenges in the full integration of power efficient CMOS radio-frequency integrated circuits (RF ICs). In addition, theparasitics of on-chip passive components that are integrated on lossy silicon substrates have made CMOS-based integrated circuits inferior to their compound-semiconductor counterparts. The parasitic effects ofon-chip interconnections play a key role in RF circuit performance, particularly as the frequency of operation increases. Neglecting these effects leads to the significant degradation in

circuit performance or even failure of operation in some cases. Furthermore, unlike transistors, miniaturization of interconnections does not improve theirperformance. This paper demonstrates the impact of metal layer resistivity and layout parasitics on an RF power amplifier (PA) and a low-noise amplifier (LNA). A nonlinear fully integrated 2.4-GHz class-E PA, with a class-F driver stage, and a 5-GHz LNA are discussed. The circuits were fabricated in a standard 0.18-£gm CMOS technology. The layouts of the presented CMOS amplifiers were designed by carefullymodeling the interconnection wires during the simulations and optimizing their widths forminimum parasitic effects and hence optimum measured circuit performance. Due to the careful layout design and interconnection optimization, the implemented amplifier circuits showed a good match between the measured and simulated performance characteristics.

- Munir M. El-Desouki, Samar M. Abdelsayed, M. Jamal Deen, Natalia K. Nikolova, and Yaser M. Haddara, The Impact of On-Chip Interconnections on CMOS RF Integrated Circuits, IEEE Transactions on Electron Devices, Vol. 56, No. 9, pp. 1882-1890, September 2009.

2008 Publications:

Experimental Demonstration of a Clock Recovery Scheme Utilizing Nonlinear Relaxation Oscillation in Directly Modulated Lasers

- An experimental demonstration was presented for a clock recovery scheme suitable for low-cost short-haul optical communications. This scheme utilizes the nonlinear relaxation oscillation in a directly modulated laser (DML), which creates clock information in modulated non-return-to-zero (NRZ) optical signals. At the receiver, an injection locked oscillator (ILO) is employed to extract and restore the clock. Eye diagrams of both received data signal and recovered clock demonstrate the capability of recovering clock from the data signal with an almost closed eye at approximately 9 Gbps.

- M. Yan, C. H. Chen, Q. Xu, and W. P. Huang, "Experimental Demonstration of a Clock Recovery Scheme Utilizing Nonlinear Relaxation Oscillation in Directly Modulated Lasers," Microwave and Optical Technology Letters, In Press (accepted 11 February 2009).

Novel Noise Parameter Determination for On-Wafer Microwave Noise Measurements

- A novel method to determine the noise parameters of receivers or device-under-tests (DUT) for on-wafer, microwave noise measurements is presented. An iterative technique is utilized, and fast convergence is achieved by the proposed impedance selection principle. This proposed method reduces the parameter variations in the conventional methods. The impact of the impedance difference on the noise parameter determination is experimentally evaluated using a DUT fabricated in a standard 90 nm CMOS technology.
- C. H. Chen, Y. L. Wang, M. Bakr, and Z. Zeng, Novel Noise Parameter Determination for On-Wafer Microwave Noise Measurements, IEEE Trans. Instrumentation & Measurement, vol. 57, issue 11, pp. 2462-2471, November 2008.

A Clock Recovery Scheme Utilizing Fiber Dispersion for Burst Mode Transmission

- A novel clock recovery scheme for burst mode (BM) transmission is proposed and analyzed. The method utilizes the characteristics of the non-return-to-zero (NRZ) signals propagating through a dispersive single mode optical fiber (SMF) at wavelength around 1550 nm to extract the clock information. The amplified photo-current carrying the generated clock information by the fiber dispersion is fed directly into the injection locked oscillator (ILO) without performing conversions between currents and voltages. The proposed scheme is investigated systematically by simulation and the trade-offs between the transmission reach and the locking time is examined. It is shown that the clock recovery method is highly effective for burst mode transmission reach of 17–38 km at 10 Gbps, which is typical of access networks.
- M. Yan, C. H. Chen, and W. P. Huang, A Clock Recovery Scheme utilizing Fiber Dispersion for Burst Mode Transmission, Journal of Optical Communications, vol. 29, issue 3, pp. 134-140, 2008

Burst-mode Clock Recovery Utilizing Relaxation Oscillation in Directly Modulated Lasers

- A novel clock recovery scheme utilizing the relaxation oscillation in a directly modulated laser (DML) for burst mode (BM) transmission is proposed for the first time. In this scheme, the DML generates the clock tone along with the transmitted non-return-to-zero (NRZ) data in the optical signal. An injection locked oscillator (ILO) is employed in the receiver to extract the clock tone and restore the clock. The proposed scheme is investigated systematically and verified by simulations with different laser modulation currents as well as some non-ideal characteristics of the system. The simulation results show that the low cost clock recovery method using an ILO in an optical link using a regular DML is highly efficient for burst-mode transmission at 10 Gbps.
- M. Yan, C. H. Chen, and W. P. Huang, Burst-mode Clock Recovery Utilizing Relaxation Oscillation in Directly Modulated Lasers, IEEE/OSA Journal of Lightwave Technology, vol. 26, no. 12, pp. 1569-1576, June 15 2008.

CMOS Imaging for Biomedical Applications

- Miniaturization of biomedical test and measurement equipment using commercial micro- and nano-fabrication technologies offers many advantages such as low cost, small size, and hence portability and incorporation of “intelligence” in photodetector image-sensing elements. However, for some biomedical applications such as disease screening or detection, these image-sensing systems must be capable of detecting very low levels of emitted light from the biological samples. Currently, either charge-coupled devices (CCDs) or photomultiplier tubes (PMTs) that are expensive, consume high power, or are bulky are used.

- In the recent past, CMOS photodetectors and imaging systems have shown that they possess adequate performance characteristics to replace CCDs or PMTs in some biomedical applications, thereby providing low power, portable, and cheap integrated bioimaging systems. This replacement has only recently become possible by the improvements in the dynamic range and sensitivity of modern CMOS photodetectors.

- This work addresses some of these advanced solutions, like novel active pixel sensors that detect ultra-low light levels, and avalanche photodiodes that are integrated in CMOS and perform single photon detection.
- N. Faramarzpour, M.M. El-Desouki, M.J. Deen, Q. Fang, S. Shirani and L.W.C. Liu, CMOS Imaging for Biomedical Applications, IEEE Potentials, Vol. 27(3), pp. 31-36 (May/June 2008).

Towards Low-cost, High-sensitivty, Integrated Biosensors

- The early detection of pathogens in a solution sample using a biosensor and associated electronics manufactured in a mainstream semiconductor process is currently attracting much research and development interests around the globe. This is primarily because such a system will be low-cost, easily manufactured, and can offer very high sensitivities, thus potentially stopping the rapid spread of diseases due to water or food contamination. In this paper, we describe our current research on the design and development of an electrolyte-insulator-semiconductor field-effect transistor to detect hybridization of target DNA oligonucleotides using functionalized probes tethered to the insulator's surface of the transistor. This biological sensor, when integrated with associated signal conditioning and processing circuits, promises high sensitivity and cheaper manufacturing costs than current labeled DNA microarray optical sensing systems.
- Invited Keynote Paper, M. J. Deen, M.W. Shinwari and R. Selvaganapathy, Towards Low-cost, High-sensitivty, Integrated Biosensors, 26th International Conference on Microelectronics (MIEL 2008), Nis, Serbia, Electron Devices Society, IEEE Press, Piscataway, NJ, pp. 307-314 (11-14 May 2008).

Silicon Radio-Frequency Integrated Circuits for Wireless and Wired Applications

- In this paper, we present and discuss several CMOS-based radio-frequency integrated circuits than can be used for wireless or wired applications. In particular, we describe five types of circuits. Two types of mixers are discussed, one targeting low-voltage (0.8V) applications and another for low phase noise direct conversion receivers. Then two designs of ultra-wideband low noise amplifiers (LNAs) using the cascade topology and special matching and filtering circuits are described. The LNAs were designed with a focus on low-voltage (0.8V) applications The performance of an integrated low-power receiver front-end is then discussed. Finally, the design of a transimpedance amplifier suitable for optical communication receivers, detailed results of bit-error-rate versus input power and the performance of a printed-circuit board based low-cost optical transmitter is presented and discussed.
- Invited Paper,, M. Jamal Deen, Munir Eldesouki, Darek Palubiak and Shiva Kumar, Silicon Radio-Frequency Integrated Circuits for Wireless and Wired Applications, German Microwave Conference – GeMiC 2008, Hamburg, Germany, pp. 156-162 (10-12 March 2008).

Wave-based Approach for Microwave Noise Characterization

- The noise behavior of a two-port is usually described through the conventional set of noise parameters Fmin, Rn, and the complex Yopt. However, noise parameters developed

using wave-based techniques also have their merit as they could offer different insights to a two-port's noise behavior. Unlike the conventional noise parameters, these wave-based noise parameters could be terminal-invariant and describe only the intrinsic noise behavior of a two-port. In this paper, several important noise parameters derived from wave-based approaches are reviewed. The derivation of each set of parameters is discussed and illustrated. The measurement approach of each set of parameters is also briefly covered.

- C. H. Chen, Y. L. Wang, and M. Bakr, "Wave-based Approach for Microwave Noise Characterization," Fluctuation and Noise Letters, vol. 8, issue 1, pp. R1-R14, March 2008.

Fully Integrated Single Photon Avalanche Diode Detector in Standard CMOS 0.18µm Technology

- Avalanche photodiodes (APDs) operating in Geiger mode can detect weak optical signals at high speed. The implementation of avalanche photodiode systems in a CMOS technology makes it possible to integrate the photodetector and its peripheral circuits on the same chip. In this work, we have fabricated APDs of different sizes and their driving circuits, in a commercial 0.18µm CMOS technology. The APDs are theoretically analyzed, measured and the results are interpreted. Excellent breakdown performance is measured for the 10µm and 20µm APDs at 10.2V. The APD system is compared to the previous implementations in standard CMOS. Our APD has a 5.5 percent peak probability of detection of a photon at an excess bias of 2V, and a 30ns dead time, which is less than the previously reported results.
- N. Faramarzpour, M.J. Deen, S. Shirani and Q. Fang, Fully Integrated Single Photon Avalanche Diode Detector in Standard CMOS 0.18µm Technology, IEEE Transactions on Electron Devices, Vol. 55(3), pp. 760-767 (March 2008).

A Clock Recovery Scheme Utilizing Fiber Dispersion for Burst Mode Transmission

- A novel clock recovery scheme for burst mode (BM) transmission is proposed and analyzed. The method utilizes the characteristics of the non-return-to-zero (NRZ) signals propagating through a dispersive single mode optical fiber (SMF) at wavelength around 1550 nm to extract the clock information. The amplified photo-current carrying the generated clock information by the fiber dispersion is fed directly into the injection locked oscillator (ILO) without performing conversions between currents and voltages. The proposed scheme is investigated systematically by simulation and the trade-offs between the transmission reach and the locking time is examined. It is shown that the clock recovery method is highly effective for burst mode transmission reach of 17–38 km at 10 Gbps, which is typical of access networks.
- M. Yan, C. H. Chen, and W. P. Huang, A Clock Recovery Scheme utilizing Fiber Dispersion for Burst Mode Transmission, Journal of Optical Communications, In Press (accepted 29 January 2008).

Burst-mode Clock Recovery Utilizing Relaxation Oscillation in Directly Modulated Lasers

- A novel clock recovery scheme utilizing the relaxation oscillation in a directly modulated laser (DML) for burst mode (BM) transmission is proposed for the first time. In this

scheme, the DML generates the clock tone along with the transmitted non-return-to-zero (NRZ) data in the optical signal. An injection locked oscillator (ILO) is employed in the receiver to extract the clock tone and restore the clock. The proposed scheme is investigated systematically and verified by simulations with different laser modulation currents as well as some non-ideal characteristics of the system. The simulation results show that the low cost clock recovery method using an ILO in an optical link using a regular DML is highly efficient for burst-mode transmission at 10 Gbps.

- M. Yan, C. H. Chen, and W. P. Huang, Burst-mode Clock Recovery Utilizing Relaxation Oscillation in Directly Modulated Lasers, IEEE/OSA Journal of Lightwave Technology, In Press (accepted 18 January 2008).

2007 Publications:

CMOS Based Active Pixel for Low-Light-Level Detection: Analysis and Measurements

- An analysis of the active pixel sensor (APS), considering the doping profiles of the photodiode in an APS fabricated in a 0.18μm standard CMOS technology, is presented. A simple and accurate model for the junction capacitance of the photodiode is proposed. An analytic expression for the output voltage of the APS obtained with this capacitance model is in good agreement with measurements and is more accurate than the previously used models. A different mode of operation for the APS based on the DC level of the output, is suggested. This new mode has better low-light-level sensitivity than the conventional APS operating mode, and it has a slower temporal response to the change of the incident light power. At 1μW/cm^2 and lower levels of light, the measured signal-to-noise ratio (SNR) of this new mode is more that 10dB higher than the SNR of previously reported APS circuits. Also, with an output SNR of about 10dB, the proposed DC level is capable of detecting light powers as low as 20nW/cm2, which is about 30 times lower than the light power detected in recent reports by other groups.
- N. Faramarzpour, M.J. Deen, S. Shirani, Q. Fang, L.W.C. Liu, F. Campos and J.W. Swart, CMOS Based Active Pixel for Low-Light-Level Detection: Analysis and Measurements, IEEE Transactions on Electron Devices, Vol. 54(12), pp. 3229-3237 (December 2007).

CMOS Photodetector Systems for Low-Level Light Applications

- In this work, we have designed, fabricated and measured the performance of three different active pixel sensor (APS) structures. These APS structures are studied in the context of applications that require low--level light detection systems. The three APS structures studied were – a conventional APS, an APS with a comparator, and an APS with an integrator. A special focus of our study was on both the signal and noise characteristics of each APS structure so the key performance metric of signal-to-noise ratio can be computed and compared. Finally, the pixel structures introduced in this work can be used for applications requiring high resolution imaging, in-pixel analog-to-digital conversion, high dynamic range and low dark current.

- Invited Paper, N. Faramarzpour, M. M. El-Desouki, M. J. Deen, S. Shirani and Q. Fang, CMOS Photodetector Systems for Low-Level Light Applications, Journal of Materials Science: Materials in Electronics (Special issue for ICOOPMA 2007), 7 journal pages, In Press (Accepted 17 October 2007).

Design Issues of a Low Power Wideband Frequency Doubler Implementation in 0.18 µm CMOS

- This paper presents design issues of a wideband, low power implementation of a frequency doubler (FD) in a commercial 0.18 µm CMOS process. The FD consists of two identical unbalanced source-coupled pairs with different width-to-length (/W///L/) ratios, whose inputs are connected in parallel and its output is taken single-ended.Amplitude and phase mismatch at the differential input are considered and it is shown that there is minimal effect on the output amplitude of the 2^nd harmonic for a 5 dB difference in input amplitude and a 45 degree difference in phase. Under matched conditions, the implemented frequency doubler can be operated at a supply voltage as low as 1 V, which corresponded to a power consumption of less than 1 mW, has a 3 dB output bandwidth of 4 GHz and a conversion gain of 2.5 dB. At a suppy voltage of 1.2 V, the frequency doubler consumed 1.32 mW, has a 3 dB output bandwidth of 3 GHz and a conversion gain of 5 dB. The phase niose degradation is 6dB in both cases. in this work can be used for applications requiring high resolution imaging, in-pixel analog-to-digital conversion, high dynamic range and low dark current.
- Rizwan Murji and M. Jamal Deen, Design Issues of a Low Power Wideband Frequency Doubler Implementation in 0.18 µm CMOS, Analog Integrated Circuits and Signal Processing, Vol. 53(1), pp. 53-62 (October 2007).

Novel Noise Parameter Determination for On-Wafer Microwave Noise Measurements

- A novel method to determine the noise parameters of receivers or device-under-tests (DUT) for on-wafer, microwave noise measurements is presented. An iterative technique is utilized, and fast convergence is achieved by the proposed impedance selection principle. This proposed method reduces the parameter variations in the conventional methods. The impact of the impedance difference on the noise parameter determination is experimentally evaluated using a DUT fabricated in a standard 90 nm CMOS technology.
- C. H. Chen, Y. L. Wang, M. Bakr, and Z. Zeng, Novel Noise Parameter Determination for On-Wafer Microwave Noise Measurements, IEEE Trans. Instrumentation & Measurement, In Press (accepted 26 September 2007).

A Flicker Noise Cancellation Technique for Low-Voltage Direct-Conversion Mixers

- A technique to reduce the low-frequency noise figure of direct-conversion mixers is presented. Unlike previous techniques, the proposed method is suitable for low-voltage and low-power applications. The results presented here demonstrate that the proposed technique can significantly improve the low-frequency noise figure of the mixer, while other performance parameters remain intact.
- S. Asgaran and M.J. Deen, A Flicker Noise Cancellation Technique for Low-Voltage Direct-Conversion Mixers, Electronics Letters, Vol. 43(19), pp. 1020-1021 (13 September 2007).

Modeling the Electrical Characteristics of FET-type Sensors for Biomedical Applications

- Selective detection of biological pathogens is of great importance in health care. Early detection of infections can help isolate diseases at earlier stages and therefore facilitates early containment and eradication. Fluorescent DNA microarrays have been used extensively to detect pathogens with specific gene expressions. Recently, gate-modified transistors (BioFETs) have been used for direct electrical detection of DNA hybridization. This paper addresses a model that describes the electrical response of the BioFET to charged DNA strands, and provides some insight on the noise characteristics as limiting factors for the sensitivity of such sensors.
- Invited Paper, M. Jamal Deen and M.W. Shinwari, Modeling the Electrical Characteristics of FET-type Sensors for Biomedical Applications, Workshop on Compact Modeling, Santa Clara, CA, 4 pages (20-24 May 2007).

Design of the Input Matching Network of RF CMOS LNAs for Low-Power Operation

- Optimum design of input matching network of CMOS low-noise amplifiers (LNAs) for low-power applications is discussed in this paper. This is done through an investigation of the effect of four different matching methodologies on the gain of radio frequency (RF) CMOS LNAs by means of compact analytical expressions. It is demonstrated that methods that convert MOSFET's input impedance to 50 Ohms for power matching are more suitable for low-power applications than methods that create a real 50 Ohms resistance at the input of the LNA, such as source inductive degeneration. As it is analytically shown, this is because the former methods enhance the gain of the LNA by a factor that is inversely proportional to MOSFET's input resistance. The impact of each matching methodology on the noise figure (NF) of the LNA is also discussed in detail and design guidelines for optimum gain-NF performance are developed using analytical models of MOSFET's noise parameters. It is demonstrated that all four methods could achieve very good noise figure values, provided that the size of active and passive components are chosen carefully based on the given guidelines. Measured results of two monolithic 5.7 GHz LNAs, designed and fabricated in a 0.18 μm CMOS technology, are also presented. The input matching networks of these LNAs are optimized for low-power operation based on the theory presented in this paper. It is experimentally shown that this optimization results in approximately 60% reduction in the DC power consumption and up to 300% improvement in the overall performance of the LNA when compared with some of the most recently published LNAs.
- Saman Asgaran, M. Jamal Deen, and Chih-Hung Chen, Design of the Input Matching Network of RF CMOS LNAs for Low-Power Operation ,IEEE Transactions on Circuits and Systems I, Vol. 54(3), pp. 544-554 (March 2007).

2006 Publications:

Study of the Electrolyte-Insulator-Semiconductor Field-Effect Transistor (EISFET) with Applications in Biosensor Design

- This paper presents a comprehensive review of the ion-sensitive field-effect transistor (ISFET) and its applications in biomolecular sensing and characterization of electrochemical interfaces. An introduction to the physics of field-effect transistors is presented, followed by a study of the properties of electrolytic solutions and electrolyte interface surface effects. Full modeling of the ion-sensitive transistor is given, followed by a survey of the different uses of the ISFET in biomedical and environmental applications. Particular attention is given to the use of the ion-sensitive transistors as replacements for microarrays in DNA gene expression analysis.
- Invited Review Paper, M. Waleed Shinwari, M. Jamal Deen and Dolf Landheer, Study of the Electrolyte-Insulator-Semiconductor Field-Effect Transistor (EISFET) with Applications in Biosensor Design, Microelectronics Reliability, 33 journal pages, In Press (Accepted October 2006).

High Frequency Noise of Modern MOSFETs: Compact Modeling and Measurement Issues

- Compact modeling of the most important high-frequency (HF) noise sources of the MOSFET is presented in this paper, along with challenges in noise measurement and deembedding of future CMOS technologies. Several channel thermal noise models are reviewed and their ability to predict the channel noise of extremely small devices is discussed. The impact of technology scaling on noise performance of MOSFETs is also investigated by means of analytical expressions. It is shown that the gate tunneling current has a significant impact on MOSFETs noise parameters, especially at lower frequencies. Limitations of some commonly used noise models in predicting the HF noise parameters of modern MOSFETs are addressed and methods to alleviate some of the limitations are discussed.
- Invited Paper, M.J. Deen, C.-H. Chen, S.. Asgaran, G. A. Rezvani, J. Tao and Y. Kiyota, High Frequency Noise of Modern MOSFETs: Compact Modeling and Measurement Issues, IEEE Trans. on Electron Devices (Special Issue on Advanced Compact Models and 45-nm Modeling Challenges), Vol. 53(9), pp. 2062-2081(September 2006).

An Approach to Improve the Signal-to-Noise Ratio of Active Pixel Sensor for Low-Light-Level Applications

- CMOS photodetectors are compact, cheap, and of low power, making them good candidates for many biomedical applications. However, many of these applications require the capability of detecting low-level light. Therefore, the noise in CMOS sensors must be carefully considered. This paper presents a detailed analysis of the signal and noise properties in active pixel sensor (APS) elements. An optimum signal-to-noise ratio (SNR) of 54 dB is achieved by varying the integration time. Based on a rigorous reset-time analysis of the APS, the dc level of the sense node is proposed as the new output signal, which is more sensitive to low-level light than existing APS techniques. By varying the reset time, an optimum SNR of 56 dB is achieved for a 30-ms integration time. This approach can achieve higher SNR for the same APS structure than the previous reports found in the literature.
- N. Faramarzpour, M.J. Deen and S. Shirani, An Approach to Improve the Signal-to-Noise Ratio of Active Pixel Sensor for Low-Light-Level Applications, IEEE Trans. on Electron Devices, Vol. 53(9), pp. 2384-2391 (September 2006).

An Analytical Method to Determine MOSFET's High Frequency Noise Parameters from 50 Ohm Noise Figure Measurements

- An analytical method, along with closed-form solutions, for extracting MOSFET's RF noise parameters is presented. This method extracts the minimum noise figure, NF_min , equivalent noise resistance, R_n , and optimum source admittance Y_opt , of MOSFET directly from a single high frequency 50-? noise figure measurement. This method can accurately predict the noise parameters of deep-submicron MOSFETs.
- S. Asgaran, M.J. Deen and C-H. Chen, An Analytical Method to Determine MOSFET's High Frequency Noise Parameters from 50 Ohm Noise Figure Measurements, IEEE Radio Frequency Integrated Circuits Symposium (RFIC-2006), San Francisco, California, pp. 341-345 (11-13 June, 2006).

Signal and Noise Modelling and Analysis of CMOS Active Pixel Sensors

- The active pixel sensor (APS) structure is the most common pixel element for photodetection systems in standard complementary metal-oxide semiconductor technology. The focus of our work is on finding functional characteristics for low-light level design. Shot, reset, thermal, and 1/f noise sources are considered in APS noise modeling. We also consider a higher-order empirical model for the p-n junction capacitance to accurately calculate the signal value. Signal-to-noise ratio curves are then determined for various values of integration time, signal level, and other design parameters. These curves can lead to the optimum operating point of the APS element.
- N. Faramarzpour, M.J. Deen, and S. Shirani, Signal and Noise Modelling and Analysis of CMOS Active Pixel Sensors, Journal of Vacuum Sci. and Tech. A (Special Issue for CSTC 2005), Vol. 24(3), pp. 879–882 (May/June 2006).

Temperature Effects in CMOS Microwave Distributed Amplifiers

- Broadband amplifiers implemented in CMOS technology offer a low-cost solution as gain elements for wideband communications systems. These components must maintain an acceptable target performance for a wide range of temperatures. We present experimental results for the gain, reflection coefficients and group delay of a broadband amplifier operating from 2 GHz to 14 GHz in the temperature range 25 °C to 125 °C. The high-frequency power gain drops by approximately 0.37 dB per every 10 °C of temperature increase, the maximum input and output refection coefficients change by less than 0.1 dB / 10 °C and the change in the input-to-output group delay is negligible over the measured temperature range. The amplifier was simulated using temperature-dependent measurement-based models for the transistors, capacitors and resistors and a single-temperature electromagnetic-simulation-based model for the inductors and interconnections. Simulated gain degradation is 0.22 dB per 10 °C, which suggests that the temperature effects on the inductors and interconnections lines are very important; however, temperature-dependent simulation is not a standard feature of electromagnetic (EM) simulators. It is thus important to include temperature effects when developing models based on EM simulations. Our results suggest that the key element to be considered is the conductor's resistivity increase with temperature.

- J.C. Ranuárez, M.J. Deen and C.H. Chen, Temperature Effects in CMOS Microwave Distributed Amplifiers, Journal of Vacuum Science and Technology A (Special Issue for CSTC 2005), Vol A24(3), pp. 831-834 (May/June 2006)

Parasitics-Aware Layout Design of a Low-Power Fully-Integrated CMOS Power Amplifier

- There is a need for efficient fully integrated CMOS power amplifiers (PAs) for very low-power implanted biomedical transceiver systems. However, the parasitics of on-silicon interconnections can cause significant degradation in the performance of radio frequency integrated circuits (RF ICs) in general and PAs in particular. In this paper, we propose a special layout design approach, which was used to design the layout of a CMOS PA. This approach relies on modeling the interconnection wires in the simulations and optimizing their widths for minimum parasitic effects and hence optimum measured circuit performance. The PA circuit is operating at 2.45 GHz and is implemented in a standard 0.18 μm CMOS process. Measurement results show that at a supply voltage of 1.4 V, the PA delivers an output power of 4.5 mW with 28.5 % power-added efficiency (PAE) and a power gain of 21.5 dB. Owing to the careful layout design and interconnection optimization, the implemented PA circuit shows good efficiency and demonstrates a good match between the measured and simulated performance characteristics.
- Samar M. Abdelsayed, M. Jamal Deen and Natalia K. Nikolova, Parasitic-aware Layout Design of a Low-power Fully Integrated Complementary Metal-Oxide Semiconductor Power Amplifier, Journal of Vacuum Science and Technology A (Special Issue for CSTC 2005), Vol A24(3), pp. 835-840 (May/June 2006).

Very Low-Voltage Operation Capability of CMOS Ring Oscillators and Logic Gates

- Operation of CMOS logic gates at low supply voltages down to 100mV and ring oscillators down to 67 mV is experimentally investigated. The measured voltage transfer characteristics of CMOS inverters and logic gates are explained using the subthreshold operation of MOS transistors. Robust control of ring oscillators allows for a tuning range of 6 decades in frequency with excellent sensitivity as low as 75mV per frequency decade at low voltages in the range from 0.2V to 0.5V, when body biasing of the MOSFETs is also used. For the present state-of-art CMOS, the simple digital CMOS cells can operate properly at supply voltages down to 0.2V, but to achieve operation at lower voltages, additional circuitry is needed to maintain the matching between p- and nMOSFETs, and the circuit complexity increases. Nevertheless, the experiments with ring oscillators demonstrated good performance of CMOS circuits down to the physical limit of 2 to 3 times the thermal voltage, while logic gates with stacked transistors need a supply of approximately 4 to 6 times the thermal voltage.
- M. Jamal Deen, Sasan Naseh, Ognian Marinov and Mehdi H. Kazemeini, Very Low-Voltage Operation Capability of CMOS Ring Oscillators and Logic Gates, Journal of Vacuum Science and Technology A (Special Issue for CSTC 2005), pp. 763-769 (May/June 2006)

Evaluation of CMOS based photodetectors for low-level light detection

- Current low-level light detection technologies for biomedical applications such as DNA Microarray sensors use charge-coupled devices or photomultiplier tubes which cannot be easily integrated with electronic circuits on a chip. CMOS image sensors do allow for the integration of photosensitive and signal processing elements on the same chip. However, more research is required if optimized low-level light detectors in standard CMOS technologies are to be developed. In this research, we have investigated different photosensitive devices including vertical, lateral and avalanche photodiodes and two floating gate-well-tied phototransistors with different gate oxide thicknesses. The photodetectors were fabricated in a commercial 0.18 μm CMOS technology and their opto-electronic characteristics measured to determine the optimum configuration for low-level light detection.
- Yasaman Ardeshirpour, M. Jamal Deen and Shahram Shirani, Evaluation of CMOS Based Photodetectors for Low-level Light Detection, Journal of Vacuum Science and Technology A (Special Issue for CSTC 2005), Vol A24(3), pp. 860-865 (May/June 2006)

High Sensitivity Detection of Biological Species via the Field-Effect High Sensitivity Detection of Biological Species via the Field-Effect

- The ability to identify different biological species in a sample is a subject of intense contemporary research. Reliable and efficient design of biological and chemical sensors using mainstream semiconductor technologies will provide even the small laboratories with the ability to detect diseases that previously could have not been done without advanced and costly equipment. Sensing the presence of DNA molecules using field-effect transistors can prove to be a better alternative to current methods such as DNA microarray technology. Here, we review the main characteristics governing the principles of operation of the BioFET. Issues that affect the sensitivity and reliability of the sensor are introduced, and a brief discussion of the noise properties of these devices is presented.
- Keynote Paper, M.J. Deen, M. Waleed Shinwari, Dolf Landheer and Gregory Lopinski, High Sensitivity Detection of Biological Species via the Field-Effect, Proceedings of the IEEE International Caribbean Conference on Devices, Circuits and Systems, Playa del Carmen, Quintana Roo, Mexico, pp. 381-385 (26-28 April 2006).

2005 Publications:

A Low-Power CMOS Class-E Power Amplifier for Biotelemetry Applications

- Designing efficient, fully integrated transceivers that could operate from very low supply voltages and for biomedical implantable electronic systems is a major challenge. This paper presents a fully integrated, 2.4 GHz class-E power amplifier (PA), with a class-F driver stage. The circuit was fabricated in a standard 0.18 μm CMOS technology. Measurement results show a maximum drain efficiency of 38 % and a maximum gain of 17 dB. When operating from a 1.2 V supply, the PA delivers an output power of 9 mW with a power-added efficiency (PAE) of 33 %. The supply voltage can go down to 0.6 V with an output power of 2 mW and a PAE of 25 %. The circuit also has a second output to test the effects of using an on-chip filter in low-power designs. This work demonstrates the feasibility of using class-E PAs for short-range, low-power applications.

- Munir M. El-Desouki, M. Jamal Deen and Yaser M. Haddara, A Low-Power CMOS Class-E Power Amplifier for Biotelemetry Applications, 35th European Microwave Conference, Paris, France, pp. 441-444 (6-8 October 2005)

A Fully Integrated Low-Power CMOS Power Amplifier for Biomedical Applications

- There is an emerging need for fully integrated power amplifiers (PAs) for very low-power implanted wireless transceivers. A fully integrated power amplifier circuit operating at 2.45 GHz is presented in this work. The layout of the circuit was designed carefully. Optimization was performed on the interconnections between the circuit components, which resulted in minimized parasitics of the on-silicon metal wires and hence very good performance. Measurement results show that at 1.4 V supply, the PA delivers an output power of 3.5 mW with a 25 % power-added efficiency (PAE) and a gain of 15.5 dB. With this performance, the circuit has proved to be well-suited for low-power biomedical implanted transceiver systems.
- Samar M. Abdelsayed, M. Jamal Deen and Natalia K. Nikolova, A Fully Integrated Low-Power CMOS Power Amplifier for Biomedical Applications, European Conference on Wireless Technology, Paris France, pp. 1715-1718 (3-4 October 2005)

Low Power CMOS Integrated Circuits for Radio Frequency Applications

- This paper presents results for a mixer, two voltage-controlled oscillators (VCOs) and a frequency doubler (FD) suitable for low power CMOS radio frequency (RF) systems. Results are first described for a mixer which uses the body terminal of the transistor as one of the inputs to down-convert a 1.9 GHz RF signal to a 250 MHz intermediate-frequency (IF) signal. Next, two VCOs are described. The first VCO is an ultra-low power oscillator designed to operate in the 2.4 GHz Industrial Scientific Medical (ISM) band with a supply of 0.4 V. The second VCO described is a fully integrated LC-tank VCO with automatic amplitude control (AAC) operating at 4 GHz. Frequency tuning for this VCO is performed by accessing the body of cross-coupled transistors of the VCO core. Finally, a wideband, low power implementation of a frequency doubler is presented. The frequency doubler consists of two identical unbalanced source-coupled pairs with different W/L ratios, whose inputs are connected in parallel and its output taken single-ended. The FD is based on the MOS transistor in saturation. All circuits were designed in a deep n-well 0.18 μm technology, allowing application of different potentials to the body of different NMOS transistors.
- Invited Paper, M. Jamal Deen, Rizwan Murji, Ahmed Fakhr, Nabeel Jafferali and Wai Leung Ngan, Low Power CMOS Integrated Circuits for Radio Frequency Applications, IEE Proceedings - Circuits, Devices and Systems, Vol. 152(5), pp. 509-522 (October 2005)

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